CLAIMS

What is claimed is:

1. A multiple dispatch processor comprising:

a plurality of instruction fetch units, each instruction fetch unit capable of fetching a stream of instructions;

a plurality of instruction decode and dispatch units each coupled to a corresponding instruction fetch unit of the plurality of instruction fetch units to receive instructions therefrom;

at least one register file coupled for storing operands;

a plurality of execution units coupled to the register file and to the instruction decode and dispatch units for performing operations on operands as directed by the plurality of instruction decode and dispatch units; and

a resource allocation unit coupled to allocate execution units among the instruction decode and dispatch units.

2. The multiple dispatch processor of Claim 1, wherein the instruction decode and dispatch units are each capable of dispatching multiple instructions in a clock cycle.

3. The multiple dispatch processor of Claim 1, wherein the plurality of execution units further comprises a plurality of multifunction execution units, each of the multifunction execution units capable of handling integer and address operations.

4. The multiple dispatch processor of Claim 3, wherein the plurality of execution units further comprises a plurality of floating point execution units.

5. The multiple dispatch processor of Claim 1, wherein the resource allocation unit dynamically allocates the execution units to instruction decode and dispatch units.

6. The multiple dispatch processor of Claim 5, wherein the resource allocation unit is capable of allocating the execution units on a priority basis, using individual priority settings for each instruction decode and dispatch unit.

7. The multiple dispatch processor of Claim 5, wherein the resource allocation unit further comprises resource available register for designating available resources.

8. The multiple dispatch processor of Claim 7, having capability of turning off a clock to functional units present in the integrated circuit but marked unavailable in the resource available register.

9. A resource allocation unit for a processor comprising apparatus for receiving resource requests from a plurality of instruction decode and dispatch units, and for granting a plurality of resources to the decode and dispatch units.

10. The resource allocation unit of Claim 9, further comprising a priority register, and where resources are granted to the decode and dispatch units according to relative priority of the decode and dispatch units.

11. The resource allocation unit of Claim 9, further comprising a resource available register, the resource available register having capability of marking particular resources of the system unavailable, and where resources marked unavailable in the resource available register are not granted to the decode and dispatch units.